



For Immediate Release

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CIRANOVA PYCELLS A KEY COMPONENT OF THE IPL STANDARD 1.0

Proven interoperable parameterized cell technology enables next generation custom IC design flows

SANTA CLARA, Calif., February 23, 2009. Ciranova, the automation technology leader for analog/mixed-signal IC physical design, today announced that its interoperable PCell technology, PyCells™, is an integral part of the just announced IPL Standard 1.0 specification. PyCell Studio™, the company's PyCell development system, is available for free download at www.ciranova.com. PyCells have been well received by the analog design community with many tapeouts to date, and are supported in most major Silicon Integration Initiative (Si2) OpenAccess-capable tools.

Today, several Integrated Device Manufacturers (IDMs) are developing PDKs using PyCells. At the 2009 Design Automation Conference, TSMC announced the 65nm iPDK which marked the first time that PyCells were deployed in a Top-5 foundry's PDK offering. In addition, to ensure the continuing availability of PyCell Studio at no cost to users, Ciranova established a source code escrow and assigned Si2 as the beneficiary in 2007.

"Ciranova PyCells are a key component of the emerging interoperable design platform that is based on OpenAccess. We will continue to collaborate with Ciranova and other industry leaders such as the IPL Alliance as part of our OpenPDK initiative", said Steve Schulz, President and CEO, Silicon Integration Initiative, Inc.

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“A standard interoperable design kit format further supports innovation and best of breed tool flows for analog/mixed-signal design,” said Michael Ma, Ciranova Vice President for Business Development and a member of the Board of Directors of the IPL Alliance. “Ciranova will continue to innovate and contribute to this cause.”

About Ciranova

Ciranova is electronic design automation (EDA) company focused on large productivity improvements in RF, analog and mixed-signal IC physical design. Complementary to existing design flows, Ciranova technology dramatically reduces the time and effort needed to develop device-level layout at both the circuit and PDK levels. Ciranova supports the Si2 OpenAccess database.