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## Intel CTO calls for graphics shift

The traditional raster graphics pipeline must go, says CTO Justin Rattner of Intel, which is pitching a shift to ray tracing to bring graphics architecture in line with the multicore road map. Article ID: 208403516

## TI bolsters its analog arsenal

Continuing its hard turn toward analog, Texas Instruments has acquired Innovative Design Solutions, which develops high-speed analog products for apps such as test and measurement. Article ID: 208403386

## NXP revs soft modem for cells

NXP is developing a multimode cellular software modem that will be capable of data downlink transfers of 150 Mbps/second. That could mean 7-minute phone downloads for HD movies. www.eetimes.eu/208403569

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# Tackling design demons

## Multithreading threatens to unravel beyond 45 nm

By Anne-Françoise Pelé

Anaheim, Calif. — EDA vendors have struggled to meet the challenge of multicore IC design by rolling out multithreading capabilities for their tools. Nonetheless, a nagging question cropped up last week at the Design Automation Conference (DAC) here: Is multithreading really the best way to exploit multicore systems effectively?

"Threads are dead," asserted Gary Smith, founder and chief analyst for Gary Smith EDA. "It is a short-term solution to a long-term problem."

At the 45-nanometer node, more and more designs reach and exceed the 100 million-gate mark. These designs break current IC CAD tools, forcing EDA vendors to develop products capable of parallel processing.

&gt;&gt; 6



## Group's 'interoperable' analog flow turns up heat on Cadence

By Mark LaPedus

Anaheim, Calif. — The once-sleepy analog EDA market is suddenly generating a lot of buzz, as a number of forces combine to advance the technology and threaten Cadence Design Systems Inc.'s stranglehold.

Ciranova, Magma, Synopsys and others are entering the revived analog EDA fray with tools that compete against Cadence's. But the biggest jolt for both the market leader and its rivals occurred last week at the Design Automation Conference (DAC) here, when Taiwan Semiconductor Manufacturing Co. Ltd. threw its weight behind a fledgling alliance and announced a major thrust in analog and mixed-signal design.

During the run-up to DAC, silicon foundry giant TSMC joined the Interoperable PDK Libraries industry alliance. The IPL group, which includes Magma, Mentor, Synopsys and other tool and intellectual-property vendors, is pushing for a standard foundry process design kit (PDK). If and when this PDK technology hits the commercial market, it will function as an "interoperable" reference flow for analog and custom IC design, backers say.

Today's PDKs are proprietary and incompatible. The

&gt;&gt; 12

## EDA business struggles against tide of negatives

By Bolaji Ojo

Precision is what the electronic design automation market is all about. And generally, customers believe EDA companies have, over the decades, invented tools that have fostered design accuracy in the semiconductor engineering community.

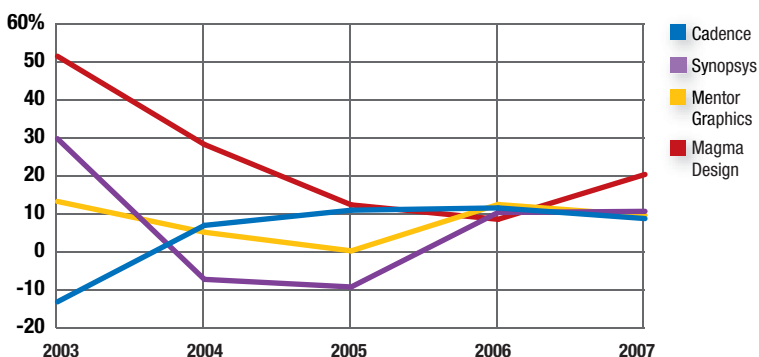
Yet, at the very moment that accolades and financial recognition should be pouring in for the industry's contributions to the rapid expansion of the high-tech market, EDA vendors are feeling more like orphans. Buffeted by the negative effects of poor and often erratic sales growth, weak leverage with customers, muddled pricing strategies and bloated operating costs, the EDA market is reeling as stockholders and private-equity investors shy away from even the better-managed companies.

What's more, in a sector where

&gt;&gt; 8

### Erratic by design

Percentage revenue growth at leading EDA companies



Source: Company data

**<<1 ANALOG** IPL-backed version is said to support analog layout tools from all vendors over a common database, and to interoperate with Cadence's proprietary analog environment.

But some view the IPL-backed flow as a competitive threat to Cadence's analog EDA tool suite, dubbed Virtuoso. Cadence has refused to join the IPL alliance, saying the rival technology provides little value for analog designers.

At DAC, the alliance got a shot in the arm when TSMC said it would offer a PDK based on the IPL technology for 65- and 45-nanometer chip designs in the first half of 2009. The foundry giant will continue to support Cadence's proprietary analog EDA environment as well. Other foundries and chip makers are expected to jump on the bandwagon, attracted by the IPL PDK's promise to reduce costs and accelerate analog/custom IC design.

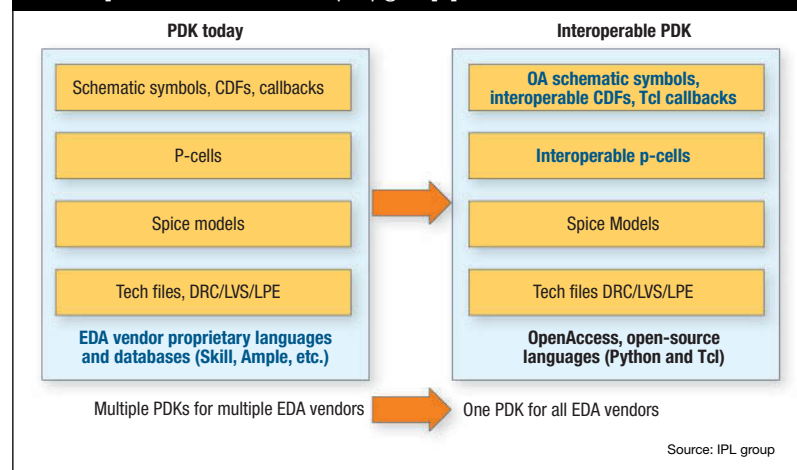
"Cadence's [analog EDA] franchise has been broken," said Gary Smith, co-founder and chief analyst with Gary Smith EDA, a market research firm.

Whereas in the past, analog EDA was "captive to one supplier," now the "world has opened up" for new and competitive tool vendors, said Aart de Geus, chief executive and chairman of Synopsys Inc.

The stakes are high in analog EDA, a \$400 million business, according to Gary Smith EDA. Cadence is estimated to own

## Proprietary vs. interoperable process design kit for analog

Interoperable PDK Libraries (IPL) group pushes standard PDK



up to an 80 percent share. Some 25 percent of Cadence's total sales are derived from custom IC tools, including analog.

There are still some major challenges in cracking Cadence's dominance. Creating an interoperable PDK sounds good on paper, but the question is whether the stodgy analog world will buy it.

With TSMC backing the IPL alliance, the technology could fly. One thing is certain: "The market is really moving toward mixed signal," said Walden Rhines, chair-

man and chief executive of Mentor Graphics Corp. "The digital chip designers are integrating more and more analog" functions on the same chip.

### Analog-digital divide

Several years ago, the digital world embraced tools that were highly automated, thereby boosting the development of complex SoC designs at competitive costs. In contrast, analog design has been stuck in the slow and painful manual world.

In simple terms, designers arrange transistor-level components—capacitors, diodes and the like—in a schematic layout. The layout is generated manually via a menu-driven programming function, based on a parameterized-cell (p-cell) methodology. The p-cell libraries include the various transistor-level components.

Cadence's Virtuoso tool suite houses the schematic-layout function, p-cell libraries and simulation tools over the industry-standard OpenAccess database. But Cadence's p-cell libraries are written in a proprietary language called Skill. This fact locks customers into Virtuoso.

Other EDA vendors sell different schematic-layout packages, bolted on top of the proprietary p-cell libraries for analog design. These tools and Cadence's do not interoperate. To read the data from one tool to another, designers must use so-called translators, which sometimes cause errors in the design flow, said Tom Quan, deputy director of design services marketing at TSMC.

That's not the only headache in analog. TSMC, for one, generated and maintained 2,500 new and different PDKs in 2007. A PDK consists of several basic elements in the analog/custom IC flow: schematic symbols and component distributed formats; p-cell libraries; Spice models; and technical files.

Each PDK is geared for a particular customer or design, but each kit is also incompatible with the others—and expensive.

Taking a step toward interoperable p-cell libraries that can be used with any OpenAccess-based IC layout tool, five EDA vendors last year formed the IPL alliance. They were Applied Wave Research, Cira-

nova, Silicon Navigator, SpringSoft and Synopsys. Others have since joined, including Helic, Jedat, Magma, Mentor, Micro Magic, Virage and, now, TSMC.

The alliance built its open-source, interoperable p-cell library upon Ciranova's PyCell Studio, a free tool that generates PyCells, or "universal" OpenAccess-based p-cells, based on a programming language called Python. PyCell Studio competes with Cadence's technology.

Late last year, the alliance expanded its charter to the development of a "standard" PDK that will operate over the OpenAccess database. Ed Lechner, director of product marketing at Synopsys and chairman of IPL, said the group has demonstrated a proof-of-concept PDK. There are reportedly no bugs with EDA tools that support the OpenAccess database. There are some issues with Magma's tools, which do not directly read OpenAccess.

The alliance claims to have tested the proof-of-concept library with Cadence's latest Virtuoso 6.1 tool. Nevertheless, it doesn't appear that Cadence will join the group. "I don't see it as a revolutionary step," said Steve Lewis, director of product marketing at Cadence. "We're not sure what the customer will derive from it."

Cadence, however, does see the value of interoperable PDKs. "Industry interoperability is a good thing," Lewis said. "For TSMC, I'm sure it's a noble cause," because "they have to do a lot of PDK development."

With regard to analog, the EDA giant is not standing still. Cadence has released a new version of Virtuoso that extends the technology for mixed-signal designs down to the 45-nm node.

### Onslaught of tools

Clearly, Cadence will get a run for its money. At DAC, Synopsys was quietly showing its new, automated analog layout tool, code-named Orion. The week before, Ciranova unveiled Helix, an automated analog layout solution. Helix's primary inputs are a Spice netlist and a PDK containing either Cadence's Skill-based p-cells or Ciranova's PyCells. The output is full device-level placement in either OpenAccess or a GDS format.

"Analog and mixed-signal design is the last major EDA market not served by automated layout methods," said Eric Filseth, Ciranova's CEO. "Up to now, the tools simply haven't delivered results acceptable to analog engineers. Helix builds on our proven PyCell technology to enable large and practical productivity gains at the full-circuit level."

Elsewhere, Helic SA launched a bond wire layout and inductance-modeling tool called VeloceWired. The tool is said to be suitable for use in the design of analog and mixed-signal ICs, where wire bond inductance may need to be considered as part of the overall component performance.

French EDA startup Infiniscale SA recently unveiled the TechYielder, for yield optimization of complex analog, advanced mixed-signal and RF blocks designed with sub-90-nm design kits. ■

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