TSMC PDK Support & Interoperable PDK libraries

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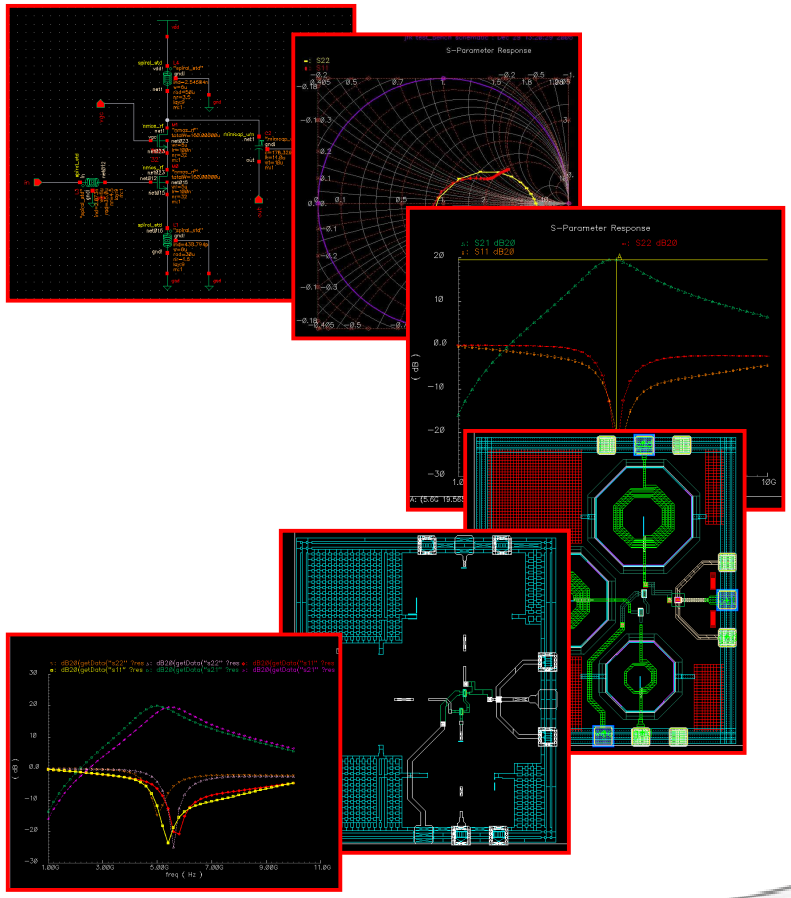
TSMC PDK Definition

TSMC Property

Process Design Kits that support a full custom design flow from schematic entry to final layout verification

- Schematic Entry
- Pre-layout Simulation
- Layout Creation
- Layout Verification (DRC, LVS, ERC)
- LPE & Post-layout Simulation
- IP or Tape Out



TSMC PDK -- Tools and Contents

Applications	Support Tools	Process Design Kits
Schematic Entry	Cadence(Composer), Mentorg(DA-IC)	Symbol, CDF, Callback, Utilities
Circuit Simulation	Cadence(AMS), Synopsys(Hspice), Cadence(Spectre), Mentorg(Eldo), Agilent(RFDE)	Models, Simulation views, Back-annotation, Dynamic-link
Layout Editor	Cadence(Virtuoso), Mentorg(IC station), SpringSoft(Laker)	Layout technology files, Pcells, Utilities, Auto route
Layout Verification (LVS/ERC/DRC)	Mentorg(Calibre), Synopsys(Hercules), Magma(Quartz)	LVS decks, LVS views, DRC decks, ERC decks, DFM utilities
Layout Parasitic Extraction (LPE)	Mentorg(Calibre XRC), Synopsys(Star-RCXT), Cadence(QRC), Magma(Quartz,Quickcap)	RC tech files, LPE decks, Mapping files for extracted view, CCI flow
Electromagnetic solver	Integrand(EMX), Ansoft (HFSS), Agilent(Momentum), Helic(VeloceRF), Cadence (VPCD), Lorentz (PV EMD), OEA (Sprial), Silvaco (Quest), Zeland(IE3D)	RCX tech file, qualification report, integration flow

TSMC PDK Selection

- Cover TSMC processes from 0.60µm to 45nm
- Cover Logic, MM, RF, SiGe, High Voltage

TSMC PDK Advanced Features

TSMC Property

- Easy Adoption
- Design Accuracy
- Design Efficiency

LNA Reference Design

TIF/TCF Analysis

Comparison of 0.18um and 65nm PDK

Items	0.18um RF	65nm RF
Device Number	125	590
Utility Number	0	16
MOS p-cell code CDF Option	10	68
QA Time	15hrs	90 hrs
MOS Call-back Function(lines)	275	4000
DRC (lines)	4016	23464
LVS (lines)	3867	25574

Challenges of PDK support ?

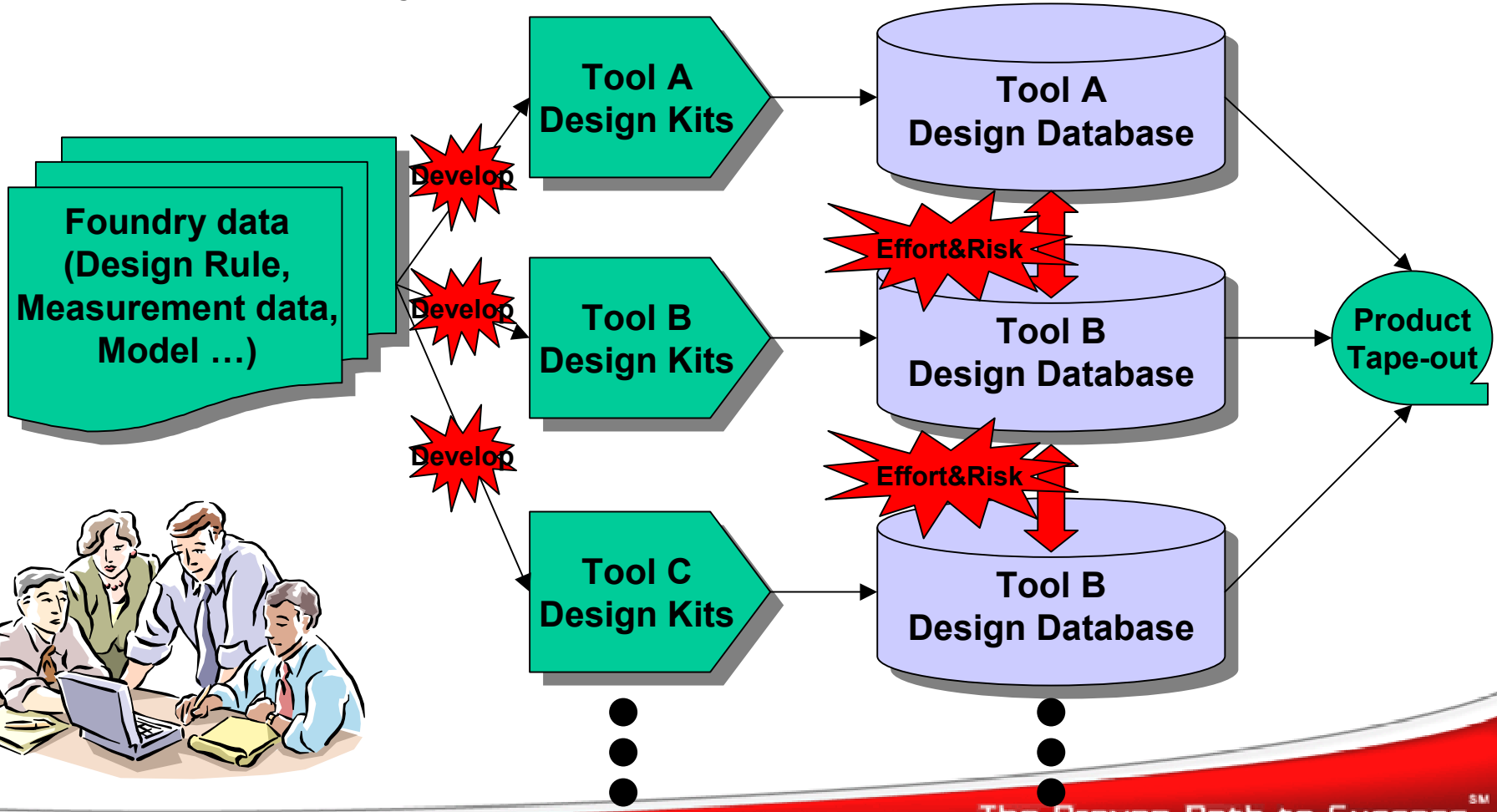
- Technologies (N32 ~ 1.0um)
- Nodes (Logic, MM/RF, HV ..)
- Applications (Schematic entry, layout edit …)
- Tools for same application (Virtuoso, IC station, Laker …)
- More and more features/complexity in advanced PDK

Over 2500 AAA (Active Accuracy Assurance) design kits released in 2007

→ Too many PDKs to support in near future

Effort and Risk in Current PDK Development

1. Effort in developing different design kits
2. Effort&Risk in using design database translation
3. Barrier for any new tools



Desired PDK Support

TSMC Property

1. Interoperable PDK can be ready earlier for current and future tools
2. No PDK barrier for changing tools
3. Seamlessly use different tools for different applications
4. Green PDK → Save resources of PDK development & design database translation

Challenges of Interoperable PDK

- Professional PDK contents
  - Are tools ready for professional PDK with basic and advanced features?
- Competitive vendors to work together forever?
  - Committee to decide new features in PDK?
- Innovation and interoperability
  - RCX tech file → table-based tools and equation-based tools
- Interoperable PDK qualification program